WWW.VIDYARTHIPLUS.COM

UNIT-1 INSTRUCTION LEVEL PARALLELISM

TWO MARK QUESTION:

1. Expand ILP?

2. What is called instruction parallelism?

3. What are the approaches to exploit ILP?

4. What is peipelining?

5. Write down the formula to calculate the pipeline CPI?

6. What is called Loop level parallelism?

7. Given the methods to enhance performance of ILP?

8. List out the types of dependences?

9. When is an instruction said to be dependent?

10. When does name dependence occur?

11. Brief on data dependence?

12. Define register renaming?

13. What is data hazard?

14. Give the classification od data hazards?

15. What is control dependence?

16. List out the constraints imposed by control dependences?

17. What are the properties used for preserving control dependence?

18. What is data flow?

19. define dynamic scheduling?

20. List the advantages if dynamic scheduling?

21. Give the idea of dynamic scheduling?

22. When an exception is said to be imprecise?

23. Why does the imprecise exception occur?

24. What are the three stages of tomasulo algorithm?

25. What are the components of hardware based speculation?

26. What is reorder buffer?

27. List out the fields in each ROB entry?

28.what is loop unrolling?

29.what are the benefits of speculating through multiple branches?

30.what is multiple issues?

31.what re abasic ideas pipeline scheduling?

32.why do we need branch prediction?

33.what are the strategies of branch predictor?

16mark question:

1.basic compiler techniques for exposing ILP

2.dynamic scheduling?

3.concepts and challenge of ILP

UNIT-2 MULTIPLE ISSUE PROCESSOR

TWO MARKS:

1.VLIW

2.Responsibilities of VLIW

3.Advantages of VLIW processor

4.EPIC

5.loop level analysis

6.classification date dependence in loops?

7.loop carried dependence?

8.not loop carried dependence?

9.when is loop level said to be parallel?

12.recurrence?

13.dependence analysis algorithm?

14.when an array index is said to be index?

15.copy propagation?

16.tree height reduction technique?

17.components of software pipeline loop?

18.Trace scheduling

19.Steps used for trace scheduling

20.How are the super blocks formed?

21.Tail duplication do?

22.Conditional moves used

23.Limitation of predicted insructions

24.IA-64 processor

25.Components of IA-64 register model

26.Register stack mechanism?

27.CFM

28.Use of CFM pointer

29.Types of register and its purpose?

30.Benefits of register rotation?

16mark question:

1.advanced compiler support for exposing and exploiting ILP

2.hardware support for exposing parallelism

3.hardware vs software speculation mechanism(8)

4.limits on ILP (8)

UNIT-3 MULTIPROCESSOR AND THREAD LEVEL PARALLELISM

TWO MARKS:

1.parallel computers?

2.idea of using multiple processors?

3.categories of Flynn's taxonomy of parallel machines

4.SMP

5.distributed memory multiprocessor

6.components of distributed memory multiprocessor

7.Benefits of distributed memory multiprocessor

8.Advantages of distributed memory multiprocessor

9.Drawbacks of distributed memory multi processor

10.Distributed shared memory

11.Address space said to be shared

12.Message passing multiprocessor

13.Multiple address space

14.Types of message passing

15.Synchronous message passing

16.Asynchronous message passing

17.Performance metrics for communication mechanisms

18.Write down the formula to calculate communication latency

19.Amdahl's law

20.Challenge of parallel processing

21.Symmetric shared memory architectures

22.Types of data cached in shared memory machines

23.Cache coherence

24.Coherent memory system

25.Memory system achieving coherent state

26.Coherence

27.Consistency

28.Cache coherence protocols

29.List out the classes of protocols

30.Directory based protocol

31.Snooping

32.What is write invalidate protocol

33.What is wrute update protocol

34.Spin locks

35.Which mechanism is used to implement spin lock

36.When is spin lock is used

37.How will be the coherence protocol is implemented

38.List out the responsibilities of controller

39.Coherency misses

40.Types of coherency misses

41.List out the techniques for implementinf the spin locks

42.Exponential backoff

43.How does a queuing lock work?

44.Consistency

45.Multithreading

46.Approaches of multithreading

16.mark question:

1.symmetric shared memory architecture

2.distributed shared memory architecture

3.multi threading(8)

4.relaxed consistency model(8)

UNIT4- MEMORY AND I/O

TWO MARK QUESTION:

1.Memory hierarchy

2.Advantage of memory hierarchy

3.Cache

4.Cache hit

5.Cache miss

6.Factors on which the cache miss depends on

7.Latency determine

8.Bandwidth determine

9.Principle of locality

10.Types of locality

11.Page fault error

12.Write down the formula to calculate cpu execution time

13.Memory stall cycles

14.Miss penalty

15.Average memory access time

16.Techniques to reduce the miss penalty

17.Technique to reduce the miss rate

18.Technique to reduce hit time

19.Technique used for improving bandwidth

20.Storage devices

21.Tracks

22.Sector

23.Sequence recorded

24.Constant bit density

25.Seek

26.Seek time

27.Average seek time

28.Rotational latency or rotational delay

29.Transfer time

16MARK QUESTION:

1.Reducing cache miss penalty,miss fail and hit time

2.Raid level

UNIT5: MULTI CORE ARCHITECTURES

TWOMARKS QUESTION:

1.Software multithreading

2.Hardware multithreading

3.Difference between software and hardware multithreading

4.Approaches in hardware multithreading

5.Simultaneous multithreading

6.Features exploit by SMT

7.Design challenge of SMT

8.Performance of SMT are improved

9.CMP

10.Chip multithreading

11.Multicore micro processor

12.Heterogeneous multicore processor

13.Advantange of heterogenous multi core processor

14.Disadvantage of heterogeneous multi core processors

15.IBM cell processor

16.Components used in IBM cell architecture

17.Components of PPE

18.Function of PPU

19.Function of PPSS

20.Intel core micro architecture

21.Block diagram of SPE

22.Components of SPE

23.Function of SPU

24.Memory flow controller

16MARK QUESTION:

1.IBM cell processor

2.SUN CMP architecture

UNIT-1 INSTRUCTION LEVEL PARALLELISM

TWO MARK QUESTION:

1. Expand ILP?

2. What is called instruction parallelism?

3. What are the approaches to exploit ILP?

4. What is peipelining?

5. Write down the formula to calculate the pipeline CPI?

6. What is called Loop level parallelism?

7. Given the methods to enhance performance of ILP?

8. List out the types of dependences?

9. When is an instruction said to be dependent?

10. When does name dependence occur?

11. Brief on data dependence?

12. Define register renaming?

13. What is data hazard?

14. Give the classification od data hazards?

15. What is control dependence?

16. List out the constraints imposed by control dependences?

17. What are the properties used for preserving control dependence?

18. What is data flow?

19. define dynamic scheduling?

20. List the advantages if dynamic scheduling?

21. Give the idea of dynamic scheduling?

22. When an exception is said to be imprecise?

23. Why does the imprecise exception occur?

24. What are the three stages of tomasulo algorithm?

25. What are the components of hardware based speculation?

26. What is reorder buffer?

27. List out the fields in each ROB entry?

28.what is loop unrolling?

29.what are the benefits of speculating through multiple branches?

30.what is multiple issues?

31.what re abasic ideas pipeline scheduling?

32.why do we need branch prediction?

33.what are the strategies of branch predictor?

16mark question:

1.basic compiler techniques for exposing ILP

2.dynamic scheduling?

3.concepts and challenge of ILP

UNIT-2 MULTIPLE ISSUE PROCESSOR

TWO MARKS:

1.VLIW

2.Responsibilities of VLIW

3.Advantages of VLIW processor

4.EPIC

5.loop level analysis

6.classification date dependence in loops?

7.loop carried dependence?

8.not loop carried dependence?

9.when is loop level said to be parallel?

12.recurrence?

13.dependence analysis algorithm?

14.when an array index is said to be index?

15.copy propagation?

16.tree height reduction technique?

17.components of software pipeline loop?

18.Trace scheduling

19.Steps used for trace scheduling

20.How are the super blocks formed?

21.Tail duplication do?

22.Conditional moves used

23.Limitation of predicted insructions

24.IA-64 processor

25.Components of IA-64 register model

26.Register stack mechanism?

27.CFM

28.Use of CFM pointer

29.Types of register and its purpose?

30.Benefits of register rotation?

16mark question:

1.advanced compiler support for exposing and exploiting ILP

2.hardware support for exposing parallelism

3.hardware vs software speculation mechanism(8)

4.limits on ILP (8)

UNIT-3 MULTIPROCESSOR AND THREAD LEVEL PARALLELISM

TWO MARKS:

1.parallel computers?

2.idea of using multiple processors?

3.categories of Flynn's taxonomy of parallel machines

4.SMP

5.distributed memory multiprocessor

6.components of distributed memory multiprocessor

7.Benefits of distributed memory multiprocessor

8.Advantages of distributed memory multiprocessor

9.Drawbacks of distributed memory multi processor

10.Distributed shared memory

11.Address space said to be shared

12.Message passing multiprocessor

13.Multiple address space

14.Types of message passing

15.Synchronous message passing

16.Asynchronous message passing

17.Performance metrics for communication mechanisms

18.Write down the formula to calculate communication latency

19.Amdahl's law

20.Challenge of parallel processing

21.Symmetric shared memory architectures

22.Types of data cached in shared memory machines

23.Cache coherence

24.Coherent memory system

25.Memory system achieving coherent state

26.Coherence

27.Consistency

28.Cache coherence protocols

29.List out the classes of protocols

30.Directory based protocol

31.Snooping

32.What is write invalidate protocol

33.What is wrute update protocol

34.Spin locks

35.Which mechanism is used to implement spin lock

36.When is spin lock is used

37.How will be the coherence protocol is implemented

38.List out the responsibilities of controller

39.Coherency misses

40.Types of coherency misses

41.List out the techniques for implementinf the spin locks

42.Exponential backoff

43.How does a queuing lock work?

44.Consistency

45.Multithreading

46.Approaches of multithreading

16.mark question:

1.symmetric shared memory architecture

2.distributed shared memory architecture

3.multi threading(8)

4.relaxed consistency model(8)

UNIT4- MEMORY AND I/O

TWO MARK QUESTION:

1.Memory hierarchy

2.Advantage of memory hierarchy

3.Cache

4.Cache hit

5.Cache miss

6.Factors on which the cache miss depends on

7.Latency determine

8.Bandwidth determine

9.Principle of locality

10.Types of locality

11.Page fault error

12.Write down the formula to calculate cpu execution time

13.Memory stall cycles

14.Miss penalty

15.Average memory access time

16.Techniques to reduce the miss penalty

17.Technique to reduce the miss rate

18.Technique to reduce hit time

19.Technique used for improving bandwidth

20.Storage devices

21.Tracks

22.Sector

23.Sequence recorded

24.Constant bit density

25.Seek

26.Seek time

27.Average seek time

28.Rotational latency or rotational delay

29.Transfer time

16MARK QUESTION:

1.Reducing cache miss penalty,miss fail and hit time

2.Raid level

UNIT5: MULTI CORE ARCHITECTURES

TWOMARKS QUESTION:

1.Software multithreading

2.Hardware multithreading

3.Difference between software and hardware multithreading

4.Approaches in hardware multithreading

5.Simultaneous multithreading

6.Features exploit by SMT

7.Design challenge of SMT

8.Performance of SMT are improved

9.CMP

10.Chip multithreading

11.Multicore micro processor

12.Heterogeneous multicore processor

13.Advantange of heterogenous multi core processor

14.Disadvantage of heterogeneous multi core processors

15.IBM cell processor

16.Components used in IBM cell architecture

17.Components of PPE

18.Function of PPU

19.Function of PPSS

20.Intel core micro architecture

21.Block diagram of SPE

22.Components of SPE

23.Function of SPU

24.Memory flow controller

16MARK QUESTION:

1.IBM cell processor

2.SUN CMP architecture

-Mr.lonely