

PART B — (5 × 16 = 80 marks)

11. (a) (i) State and prove De Morgan's theorem. (7)
(ii) Convert the following :
 $(10101011)_2 = ()_{16}$
 $(37564)_8 = ()_{10}$
 $(FACE)_{16} = ()_2$ (9)

Or

- (b) Simplify the following function using
(i) Karnaugh map (8)
(ii) Quine McCluskey method (8)
 $F(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 7, 12, 13, 14)$.
12. (a) (i) Design a full adder and implement it using only NAND gates. (8)
(ii) Design a Binary to Gray code converter. (8)

Or

- (b) (i) Design a Magnitude comparator to compare two 3-bit binary numbers. (8)
(ii) Implement the following function using suitable multiplexer.
 $F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 6, 7, 9, 10, 11)$. (8)
13. (a) (i) Explain the working of a JK flip flop with its characteristic equation, characteristic table and logic diagram.
(ii) Design a synchronous counter to count the following sequence.
0, 1, 3, 5, 7, 9, 12, 0, 1, 3,

Or

- (b) (i) Design a 3-bit universal shift register. (8)
(ii) Obtain a minimal state table using partition technique for the following state table.

Present State	Next State, Z	
	X = 0	X = 1
q_1	$q_2, 0$	$q_3, 1$
q_2	$q_6, 0$	$q_4, 1$

Present State	Next State, Z	
	X = 0	X = 1
q_3	$q_4, 1$	$q_5, 0$
q_4	$q_3, 1$	$q_6, 0$
q_5	$q_4, 0$	$q_5, 1$
q_6	$q_3, 0$	$q_5, 1$
q_7	$q_3, 0$	$q_4, 1$
q_8	$q_3, 1$	$q_1, 0$

14. (a) With suitable example, explain the steps involved in the design of pulse-mode circuits.

Or

- (b) Design a fundamental mode circuit with two-input (x_1, x_2) and one output (z) to meet the following specifications. Whenever $x_1 = 0, z = 0$. The first change in input x_2 that occurs while $x_1 = 1$ must cause the output to become $z = 1$. A $Z = 1$ output must not change to $z = 0$ until $x_1 = 0$.

15. (a) Implement the following function using :

(i) PAL

(ii) PLA.

$$f(A, B, C, D) = \sum m(0, 5, 7, 9, 11, 13, 14). \quad (8 + 8)$$

Or

- (b) (i) Explain the EPROM technology. (6)
- (ii) With schematic diagram, explain the two input TTL NAND gate operation. (10)