VALLIAMMAI ENGINEERING COLLEGE

SRM NAGAR, KATTANKULATHUR-603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

AP7202 – ASIC AND FPGA DESIGN QUESTION BANK

UNIT – I

OVERVIEW OF ASIC AND PLD

PART – A

1. Differentiate between the standard cell based ASICs and full custom ASIC.
2. Differentiate the devices PAL, PLA and FPGA.
3. What is the advantage of λ based design rule
4. Draw block diagram of the PLA.
5. How the standard cell is classified?
6. What is the impact of Moore's Law on the Semiconductor Industry?
7. Give the different types of ASIC Design Methodology.
8. Give some of the important CAD tools.
9. Differentiate between channeled & channel less gate array.
10. Differentiate between FPGA and CPLD
11. What are the different methods of programming of PALs?
12. What are the different levels of design abstraction at physical design?
13. What are macros?
14. What is Programmable Interconnects?
15. Compare Antifuse, SRAM, EPROM and EEPROM technologies with respect to erasing mechanism.
16. What is meant by CBIC?
17. How granularity of logic block influences the performance of an FPGA?
18. What is the difference between EEPROM and UVPROM technology?
19. What is meant by PREP benchmarks
20. What are several factors to improve propagation delay of standard cell?

PART – B

1. a). Explain the ASIC design flow and development flow, Give design of standard cell three input NAND gate and respective layout diagram.
   a) Write about design methodologies and design tools used for ASIC's design rules.
2. (a) Explain the internal structure of CPLD. How the output is considered to be the registered output?
   (b). Draw FPGA architecture and explain all parts of FPGA
3. (a). What is the function of LUT in FPGA? Implement the logic function: $F = X_1X_2 + X'_2X_3$ in an FPGA.(10)
   (b). Write short notes on CAD tools for ASIC construction, power dissipation in ASIC, Xilinx IO block in programmable ASIC.
4. (a). What is an ASIC? Explain different types of ASIC's.
   (b). Discuss the different types of programming technology used in FPGA design
5. (a). Explain the ASIC design flow with a neat diagram and write the difference between custom IC and standard IC?
   b) Explain in detail about PLA and PAL devices.
6. Explain the performance & characteristics for the following design styles.
   a) Standard cells.
   b) Cell based ASIC.
7. a). What are the various methodologies of FPGA? Explain the same with neat diagram?
   b). Discuss the different types of I/O cells used in programmable ASIC's
8. a). Why SRAM based FPGAs are popular when compared to other types? Explain?
   b). What is an Antifuse, with diagram explain metal-metal Antifuse.
9. a). Differentiate between the standard cell based ASIC's and gate array based ASIC.
   b). What is PLA. With a diagram explain a 4 × 3 PLA with six product terms with the help of diagram; explain the working of PAL devices with characteristics.
10. a). Explain in detail the internal organization of ROM.
    b). Explain in detail about EPROM and EEPROM technology.
11. a). Explain in details how an EPROM can be used to realize a sequential circuit.
    b). Why SRAM based FPGAs are popular when compared to other types? Explain?
12. a). Discuss the different types of programming technology used in FPGA design
    b). Discuss about multistage cell.

UNIT –II

ASIC PHYSICAL DESIGN

PART – A

1. What are the goals and objectives of system partitioning?
2. What is meant net cutset and edge cutset?
3. Define channel density and Elmore's delay.
4. What are the different algorithms used for system partitioning?
5. Write some of the iterative partitioning algorithms?
6. What is meant by group migration?
7. What is meant by timing constraints and power constraints?
8. Write the goals and objectives of floor planning?
9. Write the goals and objectives of placement?
10. What is meant by rectilinear routing?
11. Define MRST and EDIF.
12. Write some of the placement algorithm?
13. Define Hooke's law.
14. Write the abbreviations of SDF, PDEF, LEF, RSPF, PEF and DSPF.
15. What is meant by global routing and detailed routing?
16. Goals and objectives of Global routing?
17. Define the terms Circuit extraction and Back annotation.
18. What are the different design checks used in ASIC?
19. What is Timing Driven Placement and Timing Driven Routing
20. Define Core Rows and Routing Tracks

PART – B

1. a) Explain SDF (Standard Delay Format) back annotation/ SPEF (Standard Parasitic Exchange Format) timing correlation flow.

   b) How is scan DEF (Design Exchange Format) generated?
2. a) Explain about goals and objectives of floor planning.

   b) What are the various placement algorithms in ASIC design? Explain in brief any one of them.

3. a) Write pseudo code for simulated annealing method used for portioning and explain briefly.

   b) List the various partitioning methods in ASIC design. Explain in detail about Kernighan-Lin algorithm.
4. a) Explain the goals and objectives of floor planning and placement with an example.

   b) Write notes on any two of the Routing Mechanisms.
5. a) What are the various partitioning methods in design? Explain in brief any one of them.

   b) Explain in detail about global routing mechanism.
6. a) Write pseudo code for force directed placement algorithm and explain with an example.

   b) Write the sequence of global routing and explain briefly.
7. a) What are the goals and objectives of system portioning? Explain any one algorithm for partitioning.

   b) Distinguish between global routing and detailed routing.
8. a) State the goals and objectives of placement. Explain any one placement algorithm.

   b) Explain the different steps involved in ASIC construction.
9. a) Write the flow graph foe two phase routing method.

   b) Write note on H-tree based and MMM algorithm for clock routing
10. Write short notes on the following terms
    a. Standard Parasitic Extended Format (SPEF)
    b. Design Rule Checks (DRC)
    c. Electrical Rules Checks (ERC)
    d. Layout versus Schematic (LVS)
11. Explain in detail how interconnect delay model is estimated

    Explain in detail about Circuit extraction and measurement of delays

UNIT –III

LOGIC SYNTHESIS, SIMULATION AND TESTING

PART – A

1. What are the different methods of Logic Minimization?
2. Expand EDIF and illustrate the hierarchical nature of an EDIF file.
3. What are various ways of timing optimization in synthesis tools?

4. How does STA (Static Timing Analysis) in OCV (On Chip Variation) conditions done?
5. What are differences in clock constraints from pre CTS (Clock Tree Synthesis) to post CTS (Clock Tree Synthesis)?
6. What are SCOAP and BILBO?
7. What is a fault simulation? What are the various types of Fault simulation?
8. Define IDDQ Testing
9. What is ATPG and Why?
10. State the difference between the logic synthesis and simulation.
11. What is PODEM Algorithm?
12. Explain Fault coverage and Test coverage.
13. What is Built-in Self-Test (BIST)?
14. What do you understand by the term 'Half Gate ASIC'?
15. What is MTBF and MTTF?
16. Define the term controllability and observability
17. Define the term LFSR and BIST.
18. What is the difference between Procedural blocking and Non-blocking Assignments?
19. What is the difference between a gate instantiation and a module instantiation?
20. Difference between Procedural and Continuous assignment

PART – B

1. a) What do you mean by high level synthesis? What are the general steps in high level synthesis?
   b) Explain in detail about design flow of the Halfgate ASIC.
2. a) Explain in detail about PODEM algorithm with neat diagram
   b) Explain in detail about Delay and timing controls.
3. a) Explain in detail about the EDIF representation with neat diagram
   b) Explain in detail about the different types of fault models with neat diagram
4. a) Explain the different types of fault simulation with neat diagram
   b) Explain in detail about ATPG algorithm using test vectors with neat diagram
5. Write about:
   (a) Verilog and logic synthesis.
   (b) Scan design testing.
   (c) VHDL and logic synthesis.

6. Give a brief description of binary decision diagram in the context of logic level synthesis?

7. a) Distinguish between dynamic and static timing analysis.
   b) Explain how interconnect delay is estimated.
8. Write short notes on:
   (a) Low level design languages
   (b) CFI design representation.
9. Write about the following:
   (a) Global routing.
   (b) Special routing.
   (c) High level synthesis.
10. a) Define simulation and synthesis. Explain in detail about various simulation techniques used in FPGA design.
    b) Write in detail about automatic test pattern generation.
11. a) Briefly describe about Boundary Scan Test with suitable example.
    b) Explain in detail about various pre-layout and post-layout simulation Techniques.
12. a) Give an overview of Automatic Test Pattern Generation.
    b) Explain about Boundary scan Architecture design and its Routing.

UNIT –IV

FIELD PROGRAMMABLE GATE ARRAY

PART – A

1. What is meant by FPGA?
2. Draw the ACT1 logic module
3. What is the difference between Act2 and Act3 logic modules
4. Write the important input output requirements
5. What is meant by speed grading
6. Define the terms connectivity matrix, and PIP's.
7. Write some points about Actel Act interconnect architecture?
8. Define segmented channel routing?
9. Distinguish between Altera 5000 and 7000.
10. Give the XILINX Configurable Logic Block

11. What is meant by BIDA?
12. Write some points about Xilinx EPLD architecture?
13. Differentiate between Altera MAX 9000 and Altera FLEX interconnects architecture?
14. Define OEM?
15. Write File types used by the Actel Design Software?
16. Compare between Xilinx LCA, Actel Act and Altera MAX architecture?
17. Compare Schematic entry and Logic synthesis
18. Differentiate fine-grain and coarse grain.
19. Write the components present in the schematic library?
20. What are the advantages and disadvantages of FPGA compared to ASIC?

PART – B

1. a) Explain in brief about FPGA based system design? And explain one time programmable (OTP) based FPGA?

   b) Explain the basic logic programming elements of the FPGA with a suitable example?
2. a) Why SRAM based FPGAs are popular when compared to other types? Explain.

   b) Design 3-bit shift register, and implement using Xilinx XC4000 FPGA.
3. a) Explain the ACTEL ACT1 logic module and explain how to implement the following functions: (i) a 3 input NOR (ii) a half adder

   b) Describe the salient features of Xilinx LCA interconnect architecture.
4. a) Draw the Spartan-II I/O structure and explain its operation.

   b) Explain the 2-input SRAM based LUT operation with the help of a suitable diagram.
5. a) Write short note on Apex and Cyclone FPGA's.

   b) How FPGA placement and routing is different from ASIC placement and routing process.
6. a) Explain configurable logic block and Programmable routing matrix of Xilinx XC 4000 FPGA.

   b) How sequential circuit is implemented in Altera Flex 8000 FPGA.
7. a) Give the general structure of FPGA. And list the different commercial FPGA products?

   b) Explain the configurable logic block of Xilinx XC4000 FPGA.

8. Write short notes on the following:
   a) Multiple clock domains
   b) Routing architecture
   c) Xilinx vertex II architecture
   d) Test benches
9. a) Discuss in detail ASIC design approach using Xilinx based FPGA design tool.
   b) Explain about the FLEX and FLEX10000 logic array block architecture with neat diagrams.
10. a) With the help of neat sketches describe ALTERA's MAX logic series.
    b) Compare and list out the advantages of ALTERA's logic 8000 with Xilinx XC 4000.
11. a) Explain about the FPGA Advantage Tool that allows different design entries.
    b) Write short notes on any TWO
       i) Lattice PLD architecture.
       ii) Technology mapping for FPGAS
12. a) Draw and explain different design stages involved in the FPGA design flow
    b) Compare the different family members of XC4000 with respect to the CLB array size, Input Outputs and gate capacity.

UNIT – V

SYSTEM ON CHIP DESIGN

PART - A

1. Define SOC. What are motivating factors & Challenges of SOC?
2. Discuss about Choice of Architecture and typical goals of SOC.
3. List the Signal Integrity Effects in SOC Design.
4. What is Verification and Validation?
5. Write SOC architecture typical design steps.
6. What is System on Chip interconnection?
7. Define the terms "blocks", "macros", "cores" or "cells".
8. What are the principle drawbacks of SOC design and list their applications.
9. Provide an overview of how embedded software is tested and debugged
10. Identify the necessary skills needed to make a successful transition into embedded software Development.
11. Defines a core test interface between an embedded core and the system chip
12. What are the advantages, disadvantages of SOC, and IP cores?

13. What are the classes of Platforms?
14. Models and Methodology of Embedded System codesign
15. Hardware/Software codesign for application specific processor
16. Define Hardware/Software Codesign
17. List the hardware unit that must be present in the embedded systems.
18. What is CCD and list the advantages & disadvantages of CCD function
19. What is USB, USB 3.0 Bus Architecture and List the applications of USB.
20. What is Latency or Access time?

PART – B

1. a) Write a note on SOC design and verification techniques.
   b) Provide an overview of embedded software architectures.
2. a) Discuss and employ embedded software development tools
   b) Explain briefly about Hardware Software Co-Design.
3. a) Explain briefly about USB Controller Architecture.
   b) Hardware software partitioning and scheduling of codesign
4. Write short notes on the following SOC Test Challenges?
   a) Test Requirements
   b) Test Problems
   c) Test Architecture
   d) Test Methodology
5. a) Explain in detail about Core Test Wrapper and Test Access Mechanism.
   b) Explain in detail about SOC Test Architecture design and optimization.
6. a) Explain in detail about the types Configurable SOC Platform
   b) Architecture Mapping, Hardware/Software Interfaces, re-configurable logic and devices
7. a) Briefly explain an importance issue in system on chip design
   b) Explain briefly how the hardware / software co-simulation and co-synthesis issued are addressed.
8. Explain in detail about System-level HW-SW Co-design with neat block diagram.
9. a) write short notes on Digital camera operational steps
   b) Explain in detail about Bluetooth Radio Specifications and interface basics.
10. a) Explain in detail about typical steps in codesign process.
    b) Write a complete system for capturing, improving and storing digital images.

11. a) Explain in detail about modulator and demodulator principles.

    b) Explain in detail about the Dual-bus architecture Super Speed USB Communication Flow

12. Explain in detail about the SDRAM Read and write operation with Timing parameters: