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Question Paper Code : 71454

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the different addressing modes in computer instructions?

2. Give the format for double precision floating point representation?

3. Why is hardwired control preferred? What is it?

4. What is pipelining control?

5. What is cache memory?

6. Define Associative memory.

7. What are the advantages of RISC processor?

8. What is bus arbitration?

9. What is the role of a coprocessor?

10. What is the advantage of a Booth Algorithm?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the DMA organization and its advantages in processing many input/output instructions. (8)

(ii) What is meant by superscalar and vector processing? (8)

Or

(b) Discuss on the various types of interrupts in system organization?

12. (a) What is the hierarchy of memory organization? What are the speed, functionalities and cost incurred in each of these memory schemes?

Or

(b) Write short notes on multilevel memories and optical memories.

13. (a) Evaluate the performance in a pipelined computer architecture? What are various factors limiting the speed and performance of computers with this architecture and why?

Or

(b) Compare micro-programmed control and hardwired control in designing and developing the elements of a computer in respect of generating the control signals.

14. (a) Explain how multiplication is carried out using Booth's algorithm. Extend it for floating point operation. What are the advantages of modified Booth's algorithm?

Or

(b) What is look ahead carry addition? How to design combinational and sequential ALUs to handle computation on arithmetic and logic data?

15. (a) Stacks and subroutines need passing parameters through registers. Justify this statement using suitable calling program and subroutine. How I/O operations display few characters or line of characters. What are the various formats for it?

Or

(b) How the different generations evolved paving way to the present generation? What are the features of RISC and CISC processors? How do Dual and Quad processing evolved?