Reg. No. : | | | | | | | | | | | |

Question Paper Code : 98081

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2010

Elective

VLSI Design

VL 9252 — LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulation 2009)

Time : Three hours Maximum : 100 Marks

Answer ALL questions

PART A — (10 × 2 = 20 Marks)

1. Define subthreshold swing.

2. What is body effect?

3. What is meant by transistor reordering?

4. Define intrinsic delay.

5. Draw a 6 transistor SRAM cell.

6. Compare NOR type row decoder and NAND type row decoder in memories.

7. What is reconfigurable computing?

8. Implement function $AX^2 + BX + C$ using two multipliers and two adders.

9. Define signal activity.

10. Write down an algorithm to compute signal probabilities.

PART B — (5 × 16 = 80 Marks)

11. (a) (i) Derive an expression for short circuit power dissipation of a CMOS inverter. (10)

(ii) Write a short note on drain induced barrier lowering. (6)

Or

(b) (i) Explain basic principles of low power design. (8)

(ii) Discuss the various sources of power consumption in CMOS devices. (8)

12. (a) (i) Discuss the various features of technology mapping. (8)

(ii) Explain the circuit level techniques for minimization of power dissipation. (8)

Or

(b) (i) Explain the concept of state assignment for finite state machine to reduce power dissipation with example. (10)

(ii) Factoring out a common sub-expression can achieve power saving. Justify. (6)

13. (a) (i) How can power be reduced in write driver circuits and sense amplifier circuits? Explain. (10)

(ii) Differentiate MTCMOS from DTCMOS. (6)

Or

(b) (i) Explain the working of DCVS voltage level converter. (10)

(ii) Design a full adder using Adiabatic logic. (6)

14. (a) (i) How do you compute signal probability using binary decision diagrams? Discuss. (8)

(ii) Discuss methods of estimating average power in combinational circuits. (8)

Or

(b) Explain in detail about Monte Carlo method for estimating glitch power.

15. (a) (i) Elaborate on the use of pipelining and parallelism for low power. (8)

(ii) Discuss the principle of pre-computation logic for reducing power with a suitable example. (8)

Or

(b) Explain the various methods to minimize power based on software power optimization.

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