Reg. No. : | | | | | | | | | | | |

Question Paper Code: J7808

M.E. DEGREE EXAMINATION, JUNE 2010

Elective

VLSI Design

VL9252 — LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics)

(Regulation 2009)

Time : Three hours Maximum : 100 Marks

Answer ALL Questions

PART A — (10 × 2 = 20 Marks)

1. What are the factors that contribute towards power dissipation in a signal switching environment?

2. What is sub-threshold region?

3. What is signal gating?

4. How does a lower threshold transistor provide a faster transistor?

5. Why is clock signal, considered a notorious source of power dissipation in a synchronous digital chip?

6. What are the merits and demerits of a pass transistor logic synthesis system?

7. What is a strict-sense stationary process?

8. What is characterization process?

9. What is multiple-supply voltage design?

10. What are the sources of software power dissipation?

PART B — (5 × 16 = 80 Marks)

11. (a) What is the need for low power VLSI chips? Explain the various sources of dynamic and static power dissipation. (16)

Or

(b) Explain the principles and challenges in low power design. (16)

12. (a) Explain any three techniques used to reduce power at the logic level. (16)

Or

(b) What are the power reduction techniques used at circuit level? Explain how these techniques have major impact on the circuits. (16)

13. (a) Discuss the techniques used for power efficiency of clock generation and distribution. (16)

Or

(b) (i) Explain the techniques used to reduce switching activities in CMOS digital systems. (8)

(ii) Explain the low power design of a SRAM cell. (8)

14. (a) (i) Explain how power estimation is carried out in sequential logic circuits. (8)

(ii) Explain the advantages and disadvantages of gate-level power analysis. (8)

Or

(b) What is signal entropy? Explain how power is estimated using entropy. (16)

15. (a) Explain the optimization procedures for low power dissipation at the algorithm and architecture level. (16)

Or

(b) Explain the techniques used to minimize the software contribution to power dissipation. (16)

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