Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 77091

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(0.6875)_{10}$ to binary.

2. Prove the following using DeMorgan's theorem.

$$\left[(x+y)' + (x+y)'\right]' = x + y .$$

3. Implement a full adder with 4 × 1 Multiplexer.

4. Write the Data flow description of a 4-bit Comparator.

5. Give the block diagram of Master- Slave D flip-flop.

6. What is a Ring counter?

7. Compare asynchronous and synchronous sequential circuit.

8. What is a critical race condition? Give example.

9. Differentiate between EEPROM and PROM.

10. How to detect double error and correct single error?

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean expression in

(i) Sum-of-product

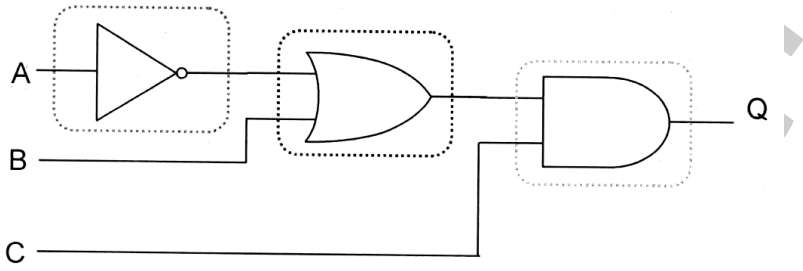
(ii) Product-of-sum using Karnaugh-map (16)

AC' + B'D + A'CD + ABCD

Or

(b) (i) Express the following function in sum of min-terms and product of max-terms $F(x, y, z) = x + yz$. (8)

(ii) Convert the following logic system into NAND gates only. (8)



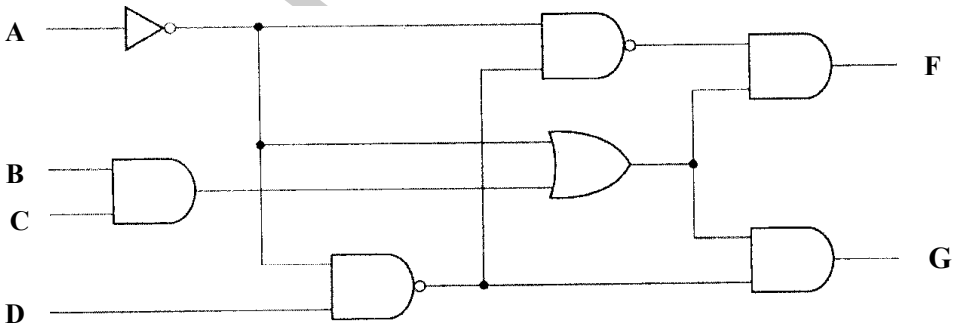
12. (a) (i) Implement the following Boolean functions with a multiplexer :

$F(w, x, y, z) = \sum (2, 3, 5, 6, 11, 14, 15)$. (8)

(ii) Construct a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoder. (8)

Or

(b) (i) Explain the Analysis procedure. Analyze the following logic diagram. (8)



(ii) With neat diagram explain the 4-bit adder with carry lookahead. (8)

13. (a) (i) A sequential circuit with two D flip-flops A and B, one input x, and one output z is specified by the following next-state and output equations :

$A(t + 1) = A' + B$, $B(t + 1) = B'x$, $z = A + B'$

(1) Draw the logic diagram of the circuit. (4)

(2) Derive the state table. (3)

(3) Draw the state diagram of the circuit. (3)

(ii) Explain the difference between a state table, characteristic table and an excitation table. (6)

Or

(b) Consider the design of a 4-bit BCD counter that counts in the following way :

0000, 0010, 0011, ..., 1001 and back to 0000.

(i) Draw the state diagram. (4)

(ii) List the next state table. (4)

(iii) Draw the logic diagram of the circuit. (8)

14. (a) (i) Explain the Race-free state assignment procedure. (8)

(ii) Reduce the number of states in the following state diagram. Tabulate the reduced state table and draw the reduced state diagram. (8)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Or

(b) Explain the hazards in combinational circuit and sequential circuit and also demonstrate a hazard and its removal with example. (16)

15. (a) (i) Write short note on Address multiplexing. (8)

(ii) Briefly discuss the sequential programmable devices. (8)

Or

(b) (i) Implement the following two Boolean functions with a PLA. (10)

F1 = A B' + A C + A' B C'

F2 = (AC + BC)'

(ii) Give the Internal block diagram of 4 X4 RAM. (6)

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