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Question Paper Code : 20414

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Fourth Semester

Electronics and Communication Engineering

EC 6404 – LINEAR INTEGRATED CIRCUITS

(Common to Medical Electronics, Robotics and Automation Engineering)

(Regulations 2013)

(Also common to PTEC 6404 – Linear Integrated Circuits for B.E. (Part-time) – Third Semester – Electronics and Communication Engineering – Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define differential mode gain.
2. State the ideal characteristics of an operational amplifier.
3. How does operational amplifier work as an integrator?
4. Draw the circuit of clipper using op-amp.
5. Mention the significances of Gilbert Multiplier cell.
6. State the various applications of phase locked loop.
7. Differentiate between direct type and integrating type in ADC converters.
8. What is the need for sample and hold circuit?
9. List the various applications of multivibrators.
10. Draw the circuit diagram of a general purpose voltage regulator.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Draw the transfer characteristics of an operational amplifier and explain its linear and non-linear operation. (8)

(ii) Discuss the operation of BJT differential amplifier with active loads. (5)

Or

(b) (i) Present the inverting and non-inverting amplifier circuits of an op-amp in closed-loop configuration. Derive the expressions for the closed-loop gain in these circuits. (9)

(ii) Define slew rate. In what way does it possess impact on the performance of an op-amp circuit? (4)

12. (a) (i) With a suitable circuit diagram, explain the operating principle of an instrumentation amplifier and derive its gain. (7)

(ii) Design a second order Butterworth low-pass filter having upper cut-off frequency of 2.1961 kHz. (6)

Or

(b) (i) Design a clipper circuit for a clipping level of +0.83V, given an input sine wave signal of 0.3 V peak. Assume the gain of the amplifier is 9 and it has an input resistance of 2.2 k-Ohm connected. (5)

(ii) Draw the operational diagram and explain the working principle of antilogarithmic amplifier and Schmitt trigger. (8)

13. (a) (i) Explain in detail on the operation of a basic phase locked loop. (5)

(ii) How are PLLs applied for frequency synthesizing and FM detection? (8)

Or

(b) (i) Obtain the expression for free running frequency of voltage controlled oscillator. (6)

(ii) Design an analog multiplier employing an emitter coupled transistor pair. (7)

14. (a) (i) Describe the operational features of R-2R ladder type D/A converter. (7)

(ii) Discuss the various switches employed for D/A converters. (6)

Or

(b) (i) With a neat block diagram, explain the operation of flash and successive approximation type A/D converter. (10)

(ii) What is oversampling? Give examples for oversampling converter. (3)

15. (a) (i) Explain the operation of an astable and monostable multivibrators with necessary diagrams. (10)

(ii) State the significant difference between fixed and adjustable voltage regulators. (3)

Or

(b) Explain the working principle and salient features of triangular wave generator and saw tooth wave generator. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a differentiator to produce an output of 6 V when the input changes by 2 V in 40 micro seconds. (5)

(ii) A PLL has a free running frequency of 600 kHz and the band-width of the low pass filter is 4 kHz. Will the loop tend to acquire lock for an input signal of 520 kHz? Explain in this case, assume that the phase detector produces sum and difference frequency components. (10)

Or

(b) (i) Design a wave generator using 555 timer for a frequency of 110 Hz and 80% duty cycle. Assume C = 0.16 μF. (7)

(ii) For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 16V.

Calculate the step change in output voltage on input varying from 0111 to 1111. (8)