EC2303 COMPUTER ARCHITECTURE AND ORGANIZATION L T P C 3 0 0 3

UNIT I INTRODUCTION 9

Computing and Computers, Evolution of Computers, VLSI Era, System Design-Register
Level, Processor - Level, CPU Organization, Data Representation, Fixed – Point Numbers, Floating Point Numbers, Instruction Formats, Instruction Types. Addressing
modes.

UNIT II DATA PATH DESIGN 9

Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division, Combinational
and Sequential ALUs, Carry look ahead adder, Robertson algorithm, booth's algorithm,
non-restoring division algorithm, Floating Point Arithmetic, Coprocessor, Pipeline Processing, Pipeline Design, Modified booth's Algorithm

UNIT III CONTROL DESIGN 9

Hardwired Control, Microprogrammed Control, Multiplier Control Unit, CPU Control Unit,
Pipeline Control, Instruction Pipelines, Pipeline Performance, Superscalar Processing,
Nano Programming.

UNIT IV MEMORY ORGANIZATION 9

Random Access Memories, Serial - Access Memories, RAM Interfaces, Magnetic Surface Recording, Optical Memories, multilevel memories, Cache & Virtual Memory,
Memory Allocation, Associative Memory.

UNIT V SYSTEM ORGANIZATION 9

Communication methods, Buses, Bus Control, Bus Interfacing, Bus arbitration, IO and
system control, IO interface circuits, Handshaking, DMA and interrupts, vectored interrupts, PCI interrupts, pipeline interrupts, IOP organization, operation systems, multiprocessors, fault tolerance, RISC and CISC processors, Superscalar and vector processor.

TOTAL= 45 PERIODS

TEXTBOOKS:

1. John P.Hayes, 'Computer architecture and Organisation', Tata McGraw-Hill, Third edition, 1998.
2. V.Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, " Computer Organisation", V edition, McGraw-Hill Inc, 1996.

REFERENCES:

1. Morris Mano, "Computer System Architecture", Prentice-Hall of India, 2000.
2. Paraami, "Computer Architecture", BEH R002, Oxford Press.
3. P.Pal Chaudhuri, , "Computer organization and design", 2nd Ed., Prentice Hall of India, 2007.
4. G.Kane & J.Heinrich, ` MIPS RISC Architecture `, Englewood cliffs, New Jersey,

2 MARKS QUESTIONS & ANSWERS

Unit – 1

1. Define Computer Architecture.

Computer Architecture deals with the structure and behavior of a computer including the information formats.

2. Define processor clock and clock rate

Processor clock:

Processor circuits are controlled by a timing signal called processor clock,the clock defines regular time interval called clock cycle.

Clock Rate:

Clock rate,R=1/p cycles/sec(hz)

Where p is length of one clock cycle

3. Explain the relation of throughput with execution and response time

Throughput:

The total amount of work done in a given time

Let us consider 2 cases:

1.) Replacing the processor in a computer with a faster version

2.) Adding additional processor to a system that uses multiple processors for separate task.

Ex:Handling an airline reservation systems.

Decreasing response time almost always improves throughput.So,in case 1 both response time & throughput increases.In case2 none of the task gets work done faster,so throughput increases.However, the demand for processing in the 2nd case was almost as large as the throughput,the system might force requests to queue up.Int this case increasing the throughput could also increase the response time,since it would decrease the waiting time in queue.Thus,in many real computer systems,changing either execution time or throughput often affects the other.

3. .Define MIPS Rate and Throughput Rate.

MIPS:

One alternative to time as the metric is MIPS(Million Instruction Per Second)

MIPS=Instruction count/(Execution time x1000000).

This MIPS measurement is also called Native MIPS todistinguish it from some alternative definitions of MIPS.

MIPS Rate:

The rate at which the instructions are executed at a given time.

Throughput:

The total amount of work done in a given time.

Throughput rate:

The rate at which the total amount of work done at a given time.

4. What is MFLOPS?What is its significant?

Popular alternative to execution time is Million Floating-point Operations Per Second ,abbreviated megaflops orMFLOPS but always pronounced “megaflops”.The formula for MFLOPS is simply the definition of the acronym:

MFLOPS=Number of floating-point operations in a program/(Execution timex1000000).

A MFLOPS rating is dependent on the program.Different programs require the execution of different number of floatin point operations.Since MFLOPS were intended to measure floating-point performance,they are not applicable outside that range.Compilers,as an extreme example,have aMFLOPS rating near 0 no matter how fast the machine is,because compilers rarely use floating-point arithmetic.

5. Define CPI

The term ClockCyclesPerInstruction Which is the average number of clock cycles each instruction takes to execute, is often abbreviated as CPI.
CPI= CPU clock cycles/Instruction count.

6. State and explain the performance equation?

Suppose that the average number of basic steps needed to execute one machine instruction is S, where each basic step is completed in one clock cycle. If the clock cycle rate is R cycles per second, the program execution time is given by
T = (N x S) / R
This is often referred to as the basic performance equation.

7. What do you mean by aligned and unaligned address?

aligned address:
· In the case of 32bit word length, natural word boundaries occur at address 0,4,8……the word locations have aligned address.
· In general, words are said to be aligned in memory if they begin at a byte address that is a multiple of the number of bytes in a word.
· FOR EXAMPLE:
If the word length is 16(2bytes), aligned words begin at byte address 0, 2, 4
unaligned address:
· There is no fundamental reason why words cannot begin at an arbitrary byte address. The words are said to have unaligned address.
While the most common case is to use aligned address, some computers allow the unaligned word address

8. What is the assembly language notation? Give example.

To represent machine instructions and program. we use assembly Language format.
For example:
The statement specifies an instruction that causes the transfer described above, from memory location LOC to processor registerR1.
Move LOC, R1
The contents of LOC are unchanged by the execution of this instruction, but the old contents of register R1 are overwritten.
The second example of adding two numbers contained in processor registers R1

and R2 and placing their sum in R3 can be specified by the assembly language statement and the assembly language statement can specify R2 and placing their sum inR3.
Add R1, R2, R3.

9. What is straight –line sequencing?
Process of fetching and executing an instruction; one at a time in order of increasing address with the help of information in program counter.

10. Specify the sequence of operation involved when an instruction is executed.
a) Instruction Fetch
b) Instruction Decode
c) Operand Fetch
d) Execute

11. what are Condition Codes (CC)? Explain the use of them.
Condition Codes are the list of possible conditions that can be tested during conditional instructions.CC is used to test the condition (<, =,>).
Based on this result, Jump instructions move to specified loop.CC flags represent the value of processor that keeps the information about the results of various operations for use by conditional branches

12. What are addressing modes?
Ø The different ways in which the location of an operand is specified in an instruction is referred to as addressing modes.
Ø It is a rule for interpreting or translating addresses field of an instruction into an effective address from where the operand is actually referenced.

13. Define absolute addressing?
Absolute addressing is defined as the operand is in a memory location. The address of this location is given explicitly in the instruction. It may also called as direct addressing.

Assembler syntax: LOC
Addressing function: EA=LOC
Where,
EA=Effective address

14. Define index mode?
Index mode is defined as the effective address of the operand is generated by adding a constant value to the contents of a register.
Symbolic Representation,
X(Ri)
Where, X is a constant value
Ri is the name of the register.
Addressing function,
EA=[Ri]+X

15. What are Number Notations?

When dealing with numerical values, it is often convenient to use the familiar decimal notation. These values are stored in the computer as binary numbers. In some situations it is more convenient to specify the binary patterns directly. Most assemblers allow numerical value to be specified in different ways.
For example the number 93 which is represented by the 8-bit binary number 01011101. If this value is to be used as an immediate operand, it can be given as a decimal number.
ADD #93, R1
or as a binary number identified by a prefix symbol such as a percent sign
ADD #%01011101, R1
Binary numbers can be written more compactly as Hexadecimal. The hex notation of a first ten pattern 0000,0001,……..1001 are represented by the digit 0,1,2……..9 as in BCD .The remaining six 4-bit patterns are represented as A,B,C,D,E,F. a hex representation is identified by a dollar sign prefix
ADD #$5D, R1

16. List out the methods used to improve system performance.

The methods used to improve system performance are

Processor clock
Basic Performance Equation
Pipelining
Clock rate
Instruction set
Compiler

17. What is Byte Addressability?

Byte Addressability is used for assigning successive memory address to successive memory location. This type of assigning is used in modern computers.
One byte=8 bits.
Ex:32bits
Address:0,4,8....

18. What is meant by Bid-Endian and Little Endian.

The name big-Endian is used when lower byte addresses are used for the most significant bytes (the left most bytes) of the word.
The name little-Endian is used when lower byte addresses are used for the less significant bytes (the right most bytes) of the word.

19. What is meant by condition codes. List out the types.

1. Negative(N)
2. Zero(Z)
3. Overflow(O)
4. Carry(C)

20. List out the additional modes used by the processor.

AutoIncrement :The Effective Address of the operand is the contents of a register specified in the instruction. After accessing the operand,the contents of a register are automatically Incremented to point to the next item in a list.
EG: (R1)+

AutoDecrement: The content of a register specified in the instruction are first automatically decremented and are then used as the effective address of the operand
EG: -(R1)

27. What do you mean by Register transfer?

Instruction execution involves a sequence of steps in which data are transferred from one register to another. For each register, two control signals are used to place the contents of that register on the bus or to load the data on the bus in to the register.
To transfer the contents of the register R1 to R4
(1)Enable the output of R1 by setting R1out to 1. This places the contents of R1 on the process bus.
(2)Enable the input of Register R4 by setting R4in to 1.This loads data from processor bus in to Register R4.

UNIT -2

1. List out rules for Booth recoded multiplier?
1. Start from LSB check each bit one by one.
2. Change the first one as -1.
3. Skip all succeeding ones (record them as zero's) until you see a zero, Change this zero as one.

2. List out the rules for mul /div of floating point number?
Multiply rule:
1. Add the exponent and subtract 127,
2. Multiply the mantissa and determine the sign of the result.
3. Normalise the resulting value, if necessary.
Divide rule:
1. Subtract the exponents and add 127,
2. Divide the mantissa and determine the sign of the result,
3. Normalise the resulting value, if necessary.

3. Write short notes on?
a) Guard bits.
b) Truncation.

4. Define the following terms.

1) Overflow
2) Underflow

Overflow:

In the single precision, if the number requires a exponent greater then +127 or in a double precision, if the number requires an exponent form the overflow occurs.

Underflow:

In a single precision ,if the number requires an exponent less than -26 or in a double presition,if the number requires an exponent less than -1022 to represent its normalized form the underflow occurs.

5. What is the principle of booth multiplication?

Booth multiplication is nothing but addition of properly shifted multiplicand patterns.

It is carried out by following steps:

a) Start from LSB. Check each bit one by one.
b) Change the first one as -1.
c) Skip all exceeding one's (record them as zeros) till you see a zero. Change this zero as one.
d) Continue to look for next one without disturbing zeros, precede using rules b), and c)

6. Convert the following binary numbers into booth recorded form.

1)11010 Booth recrded form =0-11-10
2)14 Booth recorde form=100-10.

7. List the two techniques used for speeding up the multiplication process:

The two techniques used for spreading up the multiplication process are
1)Bit pair recording or modified Booth algorithm
2)Carry save addition of summands.

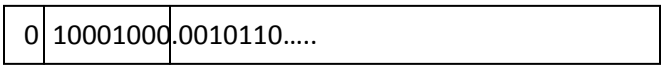
8. What are the advantages of Booth algorithm?

1. It handles both positive and negative multipliers uniformly.
2. It achieves some efficiency in the no. of additions required
When the multiplier has a few large blocks of 1's.

9. The speed gained however by skipping over 1's depends on

The data.

10. Write format for floating point in IEEE single–precision format.



Value Represented = $+0.0010110..x2^9$

a) UnNormalized Version

b) Normalized Version

11. Define n-bit ripple-carry adder.

A cascaded connection of n full adder blocks can be used to add two n-bit numbers. Since the carries must propagate or ripple, through the cascade, the configuration is called n b-bit ripple carry adder.

12. **List out the rules for add/sub of floating point number?**

1. Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents.
2. Set the exponent of the result equal to the larger exponent.
3. Perform addition /subtraction on the mantissa and determine the sign of the result.
4. Normalize the resulting value, if necessary.

Unit - 3

1. What is pipelining?

A pipelining may be visualized as a collection of segments called pipe stages through which binary information flows. Each segment performs partial processing as dictated by the task. The result obtained in each segment is transferred to the next segment in the pipeline. The final result is obtained after the data passes through all the segments.

2. Explain latency and throughput.

Latency : Each Instruction takes certain amount of time to complete. This is called as latency. It is the time differences when an instruction is issued and when it is completed.

Throughput : The number of instructions completed in a given time is called Throughput.

3. What are the major characteristics of a pipeline?

1. Pipelining cannot be implemented in a single task. As it works by splitting multiple task into a number of subtask and operating on them simultaneously.
2. The speedup or efficicenty is achieved by using the pipelining depends on the number of pipe stages and the number of available task that can be subdivide.

4. What is a pipe stage?

Each step in a pipeline is called as a pipe stage

5. what is instruction pipeline?

The type of pipeline which works by partitioning the instruction execution.

6. What are the various stages in a pipeling execution.

Instruction Fetch
Instruction Decode
Operand fetch

Opcode Execution
Write back

7. Define Pipeline Hazards?

The pipeline architectures works smoothly as long as it is able to take up new task in every machine cycle. In practice there are suitaution when the next instruction can be executed in the following machine cycle. These events called as pipeline hazards.

8. State different types of hazards that can occur in pipeline.

The types of hazards that can occur in the pipelining were,
1. Data hazards.
2. Instruction hazards.
3. Structural hazards.

Data hazards:
A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has to be delayed, and the pipeline stalls.
Instruction hazards:
The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of miss in cache, requiring the instruction to be fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.
Structural hazards:
The structural hazards is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is access to memory.

9. What is superscalar processor?

Super scalar processor exploits parallelism which has Multiple E_ Unit each of which is pipelined and it constitutes independent Instruction pipeline. The processor has PCU designed to fetch and decode several instructions concurrently which is issued to pipeline E_Units that Executes several instruction is the same.

10. What do you mean by out-of order execution? Is it Desirable?

In a pipelined processor with several instructions is process concurrently it is Possible for instruction to finish out of sequence, one instruction finishes before Another which is issued earlier. as for as main computation is concerned no Hazards will happen but if an interrupts occurs it creates the problem.

11. What are Hazards?

A hazard is also called as hurdle .The situation that prevents the next instruction in the instruction stream from executing during its designated Clock cycle. Stall is introduced by hazard. (Ideal stage)

12. List out Various branching technique used in micro program control unit?

a) Bit-Oring
b) Using Conditional Variable

c) Wide Branch Addressing

13. Compare hardwired control unit and microprogrammed control unit

Attitude
Hardwired Control
Micro Programmed control

Speed
Fast
Slow

Control function
Implemented in hardware
Implemented is software

Flexibility
Not flexible, to accommodated new system specifications or new instructions.

More flexible, to accommodate new system specifications or new instructions redesign is required.

Ability to handle large complex instruction set
Some what difficult
Easier

Ability to support.
Very difficult
Easy

Design process
Somewhat complicated
Orderly and Systematic

Applications
Mostly RISI Micro processor
Mainframes, Some Micro Processors

Instruction size

Usually under 100 instructions
Usually over 100 instructions.

Chip area Efficiency
Uses least area
Uses more Area

14. What is micro programming and micro programmed control unit?

Microprogramming is a method of control unit design in which the control unit selection and sequencing information are stored in ROM and RAM's called control store or control memory.Micro programmed control unit is a general approach used for implementation of control unit. Here control signals are generated by a program similar to machine language programs

15. What is meant by hardwired control?

. It is the one that contains control units that use fixed logic circuits to interpret instructions and generate control signals from them.

· Here, the fixed logic circuit block includes combinational circuit that generates the required control outputs for decoding and encoding functions.

16. What is the necessity of grouping signals?

· It is used to reduce the number of the bits in the microinstruction.

· It is used to overcome the drawback of assigning individual bits to each control signal results in long microinstructions, because the number of the required signals is usually large,moreoveronly a few bits are used in any given instruction.

17. List the techniques used for grouping of the control signals?

a) Vertical organization
b) Horizontal organization

18. Define Job Sequencing.

It is a process of scheduling task that are awaiting initiation in order to avoid collision and achieve high throughput.

19. Write control signals for storing a word in memory.

$R1_{out}$, MAR_{in}
$R2_{out}$, MDR_{in} ,write
$MDR_{out\ E}$, WMFC

20. What are the problems faced in Instruction Pipeline.

1. Resources Confilicts
2. Data Dependency
3. Branch Difficulties

21. What is Register Renaming?

If a temporary register assumes the role of the permanent register whose data it is holding and is given the same name is called as the Register Renaming

22. How data hazard can be prevented in pipelining?

Data hazards in the instruction pipelining can prevented by the following techniques.

· Operand Forwarding

· Software Approach

23. Explain the various approaches used to deal with Conditional pipelining?

* A condition branch instruction introduces the added hazard caused by the dependency of branch condition on result of a preceding instruction.

* Branching instruction represent about 20 percent of the dynamic interaction count of most programs.

* The dynamic count is the number of instruction execution, taking into account the that same program instruction are executed many times because of loops.

These branching junctions can le handled by following ways,

1. Delayed branch.

2. Branch prediction.

3. Dynamic branch prediction

UNIT – 4

1. What is memory system?

Every Computer contains several types of devices to store the instructions and data for its operation. These storage devices plus the algorithm implements by hardware and software needed to manage the stored information from the memory system of computer.

2. Give the classification of memory

a. Cpu Register
b. Main memory
c. Secondary Memory
d. Cache.

3. Define Static Memories and Dynamic Memories.

Memories that consist of circuits' capable of retaining their state as long as power is applied are known's static memories. In Dynamic Memories such cells do not retain their state indefinitely.

4. What is read access time?

A basic performance measure is the average time to read a fixed amount of information for instance, one word form the memory. This parameter is called the read access time.

5. Define RAM

In storage location can be accessed in any order and access time is independent of the location being accessed, the memory is termed as random access memory.

6. What is ROM?

Memories whose content cannot be altered online if they can be altered at all are read only memories.

7. What are PROMs?

Semi conductor ROMs whose contents can be changed offline-with some difficulties is called PROMs.

8. What is SRAM AND DRAM?

SRAM:Static randam access memory. It tends to be faster.they require no refreshing

DRAM:Dynamic random access memory. Data is stored in the form of charges. So continuous refreshing is needed.

9. What is volatile memory?

A memory is volatile if the loss of power destroys the stored information. Information can be stored indefinitely in a volatile memory by providing battery backup or other means to maintain a continuous supply of power.

10. What are the categories of memories,

a. SRAM
b. DRAM

11. What is flash memory.

A recent semiconductor technology called flash memory of a same non-volatility as a PROM, but it can be done a bit at a time.

12. What is cache memory?

Memory word are stored in cache data memory and are grouped into small pages called cache blocks or line. The contents of the cache's data memory are thus copies of a set of main memory blocks.

13. Mention two system organization for caches.

Two system organization for caches are
a. look aside
b. look through

14. What is RAMBUS memory?

The key feature of Rambus technology is a fast signaling method used to transfer information between chip using narrow bus.

15. What is write-through protocol?

For write operation,the cache location and the main memory location are updated simultaneously.

16. Give the difference between EEPROM and Flash memory?

The primary difference between EEPROM and flash memory is that flash restricts writes to multiple kilobytes blocks, increasing the memory capacity per chip by reducing area of control.

17. Differences between cache memory and virtual memery

1. In caches, replacement is primarily controlled by the hardware. In VM, replacement is primarily controlled by the os.
2. The Number of bits in the address determines the size of VM, where as cache size is independent of the address size.
3. But there is only one class of cache.

18. Uses of Virtual Memory.

Protection: VM is often used to protect one program from others in the system
Base and Bounds: this method allows relocation. User processes cannot be allowed to change these registers, but the OS must be able to do so on a process switch.

19. Interleaved Memory.

Banks of memory are often one word wide , so bus width need not be changed to access memory. However several independent areas of memory can be accessed simultaneously by using interleaved memory.

20. What is write back protocol?

In this scheme, only the block in cache is modified. The main memory when the block must be replaces in the cache. This requires the use of a dirty bit to keep track of blocks, that have been modified.

UNIT - 5

1. Mention the group of lines in the system bus?

*Address lines
*Data lines
*Control lines

2. What is bus master and slave master?

Input output operations involve data transfers between IO device and memory.In all the preceding operations memory is passive or slave device with respect to system bus transactions.Where as the cpu can control the system bus,i.e serve as a bus master.

3. What is the use of IO controller?

The magnetic disks and other secondary memory need to be connected to the system bus via interfacecircuits called Io controllers.
That performs series to parallel and parallel to series format conversions and other control functions.It can interface many IO device to system bus.

4. Differentiate synchronous and asynchronous communication?

In synchronous communication each item is transferred during the time slot know to both the source and destination.Data transfer is slow.

In asynchronous communication data transfer is faster and can be used for long distance communication.Each item being transferred is accompanied by the control signals.

5.What is strobe signal?

The data ready/request signals are used to load data from the source unit to the bus of from the bus to the destination unit.such control signals are called strobe signals.

6.What is bus arbitration?

The possibility exists that several master or slave units connected to a shared bus will request access to the bus at the same time.A selection mechanism called bus arbitration is therefore required to enable the current master which will still refer to a bus controller to decide among such competing request.

7.Mention the types of bus arbitration?

*Daisy chaining
*Polling
*Independent requesting

8.What is IO control method?

It refers the data transfer between the IO device and the memory or between the IO device and the cpu.eg.testing the ststus of device and to determine if they are required service by the cpu.

9.What is DMA?

The CPU and IO controller interact only when the cpu yield the control of the memory bus to the IO controller in response to the request from the latter.This level of IO control is called direct memory access and IO device interface control circuit is called DMA controller.

10.What are the advantage and disadvantages of bus?

ADV:
1.Low cost
2.Versatility.

DIS-ADV:
1.It creates a communication bottleneck
2.Limiting the maximum I/O throughput and bandwidth limitation.

11.What are the types of buses?

Processor memory bus
I/O Buses

12.what are the i/o data transfer method using memory busses

Three methods used for data transfer between io devices and cpu
1. program i/o or polling
2.interrupt driven i/o
3.direct memory access

13. Differentiate synchronous and asynchronous communication.

In Synchronous communication each item is transferred during the time slot known to both source and destination
Data transfer is slow

In Asynchronous communication data transfer is faster and can be used for long distance communication. Each item being transferred accompanied by the control signals.

14. How the interrupt is handled during exception?

* cpu identifies source of interrupt
* cpu obtains memory address of interrupt handles
* HYPERLINK "http://www.indiastudychannel.com/resources/12626-CS--Computer-Architecture-Two-marks.aspx" \t "_top"pc and other cpu status information are saved
* Pc is loaded with address of interrupt handler and handling program to handle it.

15. Difference between asynchronous bus and synchronous bus.

Synchronous bus and Asynchronous:

1. Synchronous bus on other hand contains synchronous clock that is used to validate each and every signal.

It is also synchronizing clock that is used to validate each and every signal. when it is specified clock speed is set for all time.

2 .Synchronous buses are affected noise only when clock signal occurs.

Asynchronous buses can mistake noise pulses at any time for valid handshake signal.

3. A master that receives the bus grant signal and it requesting the bus must not propagate it on down the deisgn chain.

The system control which receives the bus grant signal in VME bus .The other name for Synchronous is VME bus.

4. Synchronous bus designers must control with meta stability when attempting different clock signal Frequencies.

Asynchronous bus designer must deal with events that like synchronously.

5. Synchronous bus of meta stability arises in any flip flop. when time will be violated.

It must contend with meta stability when events that drive bus transaction.

6. Synchronous flipflop can range from nanoseconds to microseconds its range is from 20-45 nanoseconds.

When flip flop experiences effects can occur in downstream circurity unless proper design technique which are used.

16. **What is Full-HandShake**

A change of state in one signal is followed by a change in other signal. It provides the highest degree of flexibility and reliability.

17. **What is interrupt latency**?

Saving register also increases the delay between the time and interrupt request is received and state of execution of the interrupt service routine. This delay is called interrupt Latency.

18. Define Centralized Arbitration.

It means that all devices waiting to use the bus have no equal responsibility in carrying out the arbitration process.

19. Define Distributed Arbitration.

It means that all devices waiting to use the bus have equal responsibility in carrying out the arbitration process without using central arbiter.

20. Define Bus Master.

The device that is allowed to initiate data transfers on the bus at any given time

Unit -1
BASIC STRUCTURES OF COMPUTERS

1. Explain the basic functional units of a simple computer. (16)
2. Explain the basic I/O operations of modern processors. (16)
3. Write briefly about stack and quue.
4. Explain various addressing modes found in modern processors (16)
5. Explain various assembler directives used in assembly language program (08)
6. Discuss various issues to be considered while assigning the ISA of a processor 08)
7. What are stack and queues? Explain its use and give its differences (10)
8. Write a assembly language to find the biggest number among given three numbers (06)
9. Describe detail about instruction and instruction sequencing (16)
10. Describe detail about the performance of the system.(16)

Unit -2
ARITHMETIC UNIT

1. (a)Discuss the principle of operation of carry-look ahead adders. (08)
   (b)Discuss the non-restoring division algorithm. (08)
2. (a) Multiply the following pair of signed 2's complements numbers using bit pair recoded multiplier: Multiplicand = 110011 Multiplier = 101100. (08)
   (b)Describe the algorithm for integer division with suitable example. (08)
3. With a neat sketch, Explain in detail about logic design for fast adders. (16)
4. Describe how the floating-point numbers are represented and used in digital arithmetic operations. Give an example. (16)
5. (a) Explain the representations of floating point numbers in detail. (06)
   (b) Give the block diagram of the hardware implementation of addition and subtraction of signed number and explain its operations. (10)
6. (a) Design a multiplier that multiplies two 4-bit numbers. (06)
   (b) Explain the working of floating point adder and subtractor. (10)
7. Explain the Booth Algorithm for multiplication of Signed two's Complement number

Unit - 3
BASIC PROCESSING UNIT

1. Give the organization of typical hardwired control unit and explain the functions performed by the various blocks. (16)
2. Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. (16)
3. Explain in detail about instruction execution characteristics. (16)

4. With a neat block diagram, explain in detail about micro programmed control unit and
Explain its operations. (16)
5. (a)Explain the execution of an instruction with diagram. (08)
(b) Explain the multiple bus organization in detail. (08)
7. (a) Explain the function of a six segment pipeline showing the time it takes to process
eight tasks. (10)
(b) Highlight the solutions of instruction hazards. (06)
8. (a)Explain the instruction cycle highlighting the sub-cycles and sequence of steps to
be followed. (08)
(b)Illustrate memory read and write operation. (08)
9. Explain the concept of Superscalar Architecture.
10. Describe the basic structure of the pipeline processor and explain how it carried out
in floating point adder.
11. Given the sequence of control signals to be generated to fetch an instruction from memory in a single-bus organization

Unit - 4
MEMORY SYSTEM

1. Discuss the various mapping techniques used in cache memories. (08)
2. (a)Explain the concept of virtual memory with any one virtual memory management
technique. (08)
(b)Give the basic cell of an associative memory and explain its operation. Show how associative memories can be constructed using this basic cell. (08)
3. Give the structure of semiconductor RAM memories. Explain the read and write operations in detail. (16)
4. (a)Explain the organization of magnetic disks in detail. (08)
(b)Write a short note on PCI (08)
5 Explain the concept of memory hierarchy. (06)
6. Explain about the secondary storage devces
7. Describe the performance consideration of cache memory.
8. Give the structure of semiconductor ROM memories. Explain read and write operation.
9. Explain the virtual memory address translation and TLB with necessary diagram.
10. Explain the basic concepts of memory system.

Unit - 5
I/O ORGANIZATION

1. Explain the functions to be performed by a typical I/O interface with a typical input output interface. (16)
2. (a)Discuss the DMA driven data transfer technique. (08)
(b)Discuss the operation of any two input devices (08)

3. Explain in detail about interrupt handling. (16)
4. Explain in detail about standard I/O interface. (16)
5. Describe the functions of SCSI with a neat diagram. (16)
6. (a)What is the importance of I/O interface? Compare the features of SCSI and PCI Interfaces.(08)
(b) Explain the use of vectored interrupts in processes. Why is priority handling desired in interrupt controllers? How does the different priority scheme work? (08)
7. Write note on the following.
    - Bus arbitration
    - Printer process communication
    - USB
    - DMA (16)
8. Explain how DMA transfer is accomplished with a neat diagram.
9. Write short notes on,
    i)PCI
    ii)SCSI
10. Describe Bus Arbitration.
11. Explain the use of vectored interrupts in processors. Why is priority handling desired in interrupt controllers? How do the priority schemes work?